REMARKS:

This is the preliminary amendment of the above-referenced application. Applicant amends claims 1, 3 and 6 of the present application; marked up versions of the amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). Applicant adds new claim 15 to the present application. Pursuant to this amendment, claims 1-6 and 15 are pending. Reexamination and reconsideration of the application are respectfully requested.

In the Office Action dated January 4, 2001, the Examiner rejected claims 1-6 as indefinite. Applicant amends claims 1, 3 and 6 to address this rejection. The Examiner rejected claims 1-2 as anticipated by U.S. Patent No. 5,748,179 to Ito *et al.* The Examiner rejected claims 1-5 as obvious over U.S. Patent No. 5,247,375 to Mochizuki *et al* in view of U.S. Patent No. 5,187,604 to Taniguchi *et al*, the Ito patent, U.S. Patent No. 5,811,318 to Kweon, and U.S. Patent No. 5,777,702 to Wakagi *et al.* The Examiner rejected claims 1-6 as obvious over U.S. Patent No. 5,701,167 to Yamazaki *et al* in view of the Taniguchi patent, the Ito patent, the Kweon patent, and the Wakagi patent. Applicant respectfully traverses these rejections and submits that all pending claims are in condition for allowance.

The present application describes an LCD device having a plurality of pixel electrodes arranged in a matrix on a substrate and a plurality of TFT devices respectively connected to each of the plurality of pixel electrodes as the switching elements. According to the present application, one or more conductive section is/are formed on the substrate to prevent deterioration of element characteristics due to the static electricity generated during the manufacturing of the LCD device. FIGs. 1-3 of the present application illustrate the first embodiment of the present invention. In this embodiment, at least one of the wires connected to the drain driver 5 (e.g., the video data feeding wire 53, the horizontal start pulse feeding wire 52, or the horizontal clock pulse feeding wire 51) is arranged detouring around outside of the drain driver 5. An electric shielding wire 10 is formed at least on the detouring part of the selected wire(s) around outside of the drain driver 5.

Accordingly, static electricity generated during the manufacturing process will be absorbed by the electric shielding wire 10 so that damage to the elements of the drain driver 5 can be prevented. See Application, page 12, line 25—page 13, line 25.

The electric shielding wire 10 includes wire pedestal 111 formed on the substrate 100, gate insulating film 102 covering the wire pedestal 111, injection stopper 104 formed on the gate insulating film 102, interlayer insulating film 105 covering the injection stopper 104 and the gate insulating film 102, wire 116 formed on the interlayer insulating film 105 and contacting the wire pedestal 111 via an opening, and flattening insulating film 108. See Application, page 10, line 17-page 12, line 24. As shown in FIG. 3, the wire 10 that provides electric shielding protection to the drain driver 5 includes a lamination structure with two conductive layers (wire pedestal 111 and wire 116). Moreover, no additional manufacturing step is required to form the electric shielding wire 10. Specifically, the wire pedestal 111 is formed with the gate electrode 101 and the input terminal pedestal 121 as the first conductive layer. The wire 116 is formed with the input terminal contact film 129 and the source and drain electrodes 106, 107 of the TFTs as the second conductive layer. Manufacturing costs of the LCD device, therefore, will not be increased.

The Ito patent, on the other hand, describes a flip-chip style LCD device that can reduce the resistance between a flexible board and a driving IC, and at the same time can enhance resistance-to-electrocorrosion of the input wires to the driving IC. The Ito's LCD device includes plural input wires (Td) provided on the surface of the one substrate at the side of the liquid crystal layer to connect output terminals of the flexible board to input terminals of the liquid crystal driving circuits. Each input wire includes a first metal layer (g1) in the vicinity of the surface of the substrate, a transparent conductive layer (d1) laminated on the first metal layer, a second metal layer (d2) laminated on the transparent conductive layer and connected to the first metal layer at the opening portions, and a protection film (PSV1) covering at least the second metal layer. The Ito patent,

however, does not describe an electric shielding wire with a lamination structure of two or more conductive layers formed of two or more layers used to form the thin film transistors. Thus, the present application distinguishes over the Ito patent.

Similarly, none of the Mochizuki patent, the Taniguchi patent, the Kweon patent, the Wakagi patent, and the Yamazaki patent describes an electric shielding wire with a lamination structure of two or more conductive layers formed of two or more layers used to form the thin film transistors. Thus, the present application distinguishes over all of the above-mentioned patents.

Claim 1 of the present application recites, in pertinent part, "wires for sending the signal voltage from the plurality of input terminals to the plurality of thin film transistors, at least a portion thereof having a lamination structure comprising two or more conductive layers formed of two or more layers used to form the thin film transistor". As discussed, none of the Ito patent, the Mochizuki patent, the Taniguchi patent, the Kweon patent, the Wakagi patent, and the Yamazaki patent describes this limitation of claim 1. Thus, claim 1 distinguishes over the Ito patent, the Mochizuki patent, the Taniguchi patent, the Kweon patent, the Wakagi patent, and the Yamazaki patent, and is in condition for allowance.

Claim 2 depends from claim 1. Thus, claim 2 similarly distinguishes over the Ito patent, the Mochizuki patent, the Taniguchi patent, the Kweon patent, the Wakagi patent, and the Yamazaki patent, and is in condition for allowance.

Claim 3 recites, in pertinent part, "wires for connecting the plurality of driving thin film transistors and the plurality of input terminals, at least a portion thereof having a lamination structure comprising two or more conductive layers formed of two or more layers included in each switching thin film transistor and/or each driving thin film transistor". As discussed, none of the Ito patent, the Mochizuki patent, the Taniguchi patent, the Kweon patent, the Wakagi patent, and the Yamazaki patent describes this limitation of claim 3. Thus, claim 3 distinguishes over the Ito patent, the Mochizuki patent, the Taniguchi patent, the

Kweon patent, the Wakagi patent, and the Yamazaki patent, and is in condition for allowance.

Claims 4 and 5 depend from claim 3. Thus, claims 4 and 5 similarly distinguish over the Ito patent, the Mochizuki patent, the Taniguchi patent, the Kweon patent, the Wakagi patent, and the Yamazaki patent, and are in condition for allowance.

Claim 6 recites, in pertinent part, "a plurality of input terminals for receiving a control signal for driving the plurality of driving thin film transistors, having a lamination structure comprising two or more conductive layers formed of two or more layers included in each switching thin film transistor and/or each driving thin film transistor, and situated 0.8 mm or further from the plurality of driving thin film transistors". None of the Ito patent, the Yamazaki patent, the Taniguchi patent, the Kweon patent, and the Wakagi patent describes this limitation of claim 6. Thus, claim 6 distinguishes over the Ito patent, the Yamazaki patent, the Taniguchi patent, the Kweon patent, and the Wakagi patent, and is in condition for allowance.

The new claim 15 recites, in pertinent part, "wires for sending the signal voltage from the plurality of input terminals to the plurality of thin film transistors, at least a portion thereof having a lamination structure comprising two or more conductive layers formed of two or more layers used to form the thin film transistor, wherein each of the wires includes a first conductive layer formed of the lowest conductive layer of the thin film transistor and a second conductive layer situated above the first conductive layer and formed of other conductive layer of the thin film transistor". Applicant submits that the new claim 15 distinguishes over the art of record and is in condition for allowance.

The art made of record but not relied upon by the Examiner has been considered. However, it is submitted that this art neither describes nor suggests the presently claimed invention.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: July 24, 2001

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Version with markings to show changes made:

1. (Amended) A display apparatus having a plurality of pixels, comprising on a substrate:

a plurality of pixel electrodes corresponding to respective pixels among the plurality of pixels[,];

a plurality of thin film transistors, each comprising a plurality of conductive layers, for controlling supplying of signal voltage to the plurality of pixel electrodes[,];

a plurality of input terminals for receiving a control signal for the signal voltage to be supplied to the plurality of thin film transistors; and

wires for sending the signal voltage from the plurality of input terminals to the plurality of thin film transistors, at least a portion thereof having a lamination structure comprising two or more conductive layers formed of two or more layers used to form the [corresponding to a plurality of conductive layers constituting each] thin film transistor.

3. (Amended) A display apparatus having a plurality of pixels, comprising on a substrate:

a plurality of pixel electrodes corresponding to respective pixels among the plurality of pixels[,];

a plurality of switching thin film transistors, each comprising a plurality of conductive layers, connected to the plurality of pixel electrodes, for supplying signal voltage to the plurality of pixel electrodes;

a plurality of driving thin film transistors, each comprising a plurality of conductive layers, arranged close to peripheral area of the plurality of pixel electrodes, for generating a driving signal for driving the number of switching thin film transistors;

a plurality of input terminals for receiving a control signal for driving the plurality of driving thin film transistors; and

wires for connecting the plurality of driving thin film transistors and the plurality of input terminals, at least a portion thereof having a lamination structure comprising two or more conductive layers [similar to the plurality of conductive] formed of two or more layers included in each switching thin film transistor and/or each driving thin film transistor.

6. (Amended) A display apparatus having a plurality of pixels, comprising on a substrate:

a plurality of pixel electrodes corresponding to respective pixels among the plurality of pixels[,];

a plurality of switching thin film transistors, each comprising a plurality of conductive layers, connected to the plurality of pixel electrodes, for supplying signal voltage to the plurality of pixel electrodes;

a plurality of driving thin film transistors, each comprising a plurality of conductive layers, arranged close to peripheral area of the plurality of pixel electrodes, for generating a driving signal for driving the number of switching thin film transistors;

wires for connecting the plurality of driving thin film transistors and [the] a plurality of input terminals; and

a plurality of input terminals for receiving a control signal for driving the plurality of driving thin film transistors, having a lamination structure comprising two or more conductive layers [similar to the plurality of conductive] formed of two or more layers included in each switching thin film transistor and/or each driving thin film transistor, and situated 0.8 mm or further from the plurality of driving thin film transistors.